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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,044	04/08/2004	Robert Allan Faust	AUS920040056US1	9661

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EXAMINER	
NGUYEN, VINH P	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,044	FAUST, ROBERT ALLAN	
	Examiner	Art Unit	
	VINH P. NGUYEN	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8-10 and 19* is/are rejected.

7)☒ Claim(s) *2,4-7 and 11-18,20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-20 are objected to because of the following informalities:

In claims 1,10 and 19, it is what is meant by " pulses that are a first length" and pulses that are a second length" and how they are formed. Furthermore, it is unclear what "logical ones using pulses that are a first length" and "logical zeros pulses that are a second length" comprises of.

In claim 1,10 and 19, it is unclar how "data" is interrelated and associated with "logical ones" and "logical zeros"

The dependent claims not specifically address share the same indefiniteness as they depend from objected base claims.

Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1,3,8-10,12 and 19 are rejected under 35 U.S.C. 102(a) as being anticipated by Frankowsky (Pat # 6,651,203).

As to claims 1, 10,12,Frankowsky discloses an apparatus for testing the memory device (102) with a plurality of I/O pins (DQ) as shown in figure 2 having at least one input/output pin (DQ) configured to be used to transmit and receive data, an external device (,110,108) for communicating with the device (102) utilizing logic signal (one "high" or low "zero") (see column 4, lines 20-31) by transmitting the logic signal to the device utilizing the I/O pin (DQ). It

appears that the logical ones (high) in the device of Frankowsky inherently use pluses that are a first length and a logical zeros (low) in the device of Frankowsky inherently use pulses that are a second length.

As to claim 3, the external device (108,110) of Frankowsky is used fro generating the logical ones and logical zeros and it is coupled to the device (102) using the I/O pin (DQ).

As to claim 8, it appears that the external tester (110) of the external device (108,110) inherently includes a bidirectional driver in order to transmit and receive the signals from the device under test (102) and a first node (any output terminals of the tester "110") connected to that bidirectional driver and is also connected to a first communication pin (one of the terminals labeled as "data out") of the external device (108,110).

As to claim 9, the logical ones and zeros are generated by the external device (108,110) and outputted them using the first communication pin (one of the terminals labeled as "data out")

4. Claims 2,4-7, 11-18 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the Iimitations of the base claim and any intervening claims.

The prior art does not the step of configuring said 1/0 pin by connecting said 1/0 pin to a first node of a pull-up resistor and connecting a second node of said pull-up resistor to a power source; and said 1/0 pin being configured as an open collector output that will serve as both an input pin and an output as recited in claim 2.

The prior arts of record fails to disclose the steps of: connecting a first node of a second resistor included within said external device to a power source; connecting a second node of said second resistor to a first node of an LED,connecting a second node of said LED to a first communication pin of said external device; connecting said second node of said LED to a first node of a switch and connecting a second node of said switch to ground as recited in claim 4. Claims 5-7 depend from claim 4, these claims are also objected.

The prior art fails to teach an 1/0 pin being configured by connecting said 1/0 pin to a first node of a pull-up resistor and connecting a second node of said pull-up resistor to a power source; and said I/O pin being configured as an open collector output that will serve as both an input pin and an output pin as recited in claim 11.

The prior art fails to teach a first node of a second resistor included within said external device connected to a power source; a second node of said second resistor connected to a first node of an LED; a second node of said LED connected to a first communication pin of said external device; said second node of said LED connected to a first node of a switch; and a second node of said switch connected to ground as recited in claim 13. Since claims 14-18 depend from claim 13, they are also objected.

The prior art fails to teach instructions for generating a bit stream by repeatedly opening and closing a switch that is external to said device and connected to said 1/0 pin to generate

said logical ones and said logical zeros; instructions for generating said logical ones by closing said switch for a first length of time; and instructions for generating said logical zeros by closing said switch for a second length of time as recited in claim 20.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dukes et al (Pat # 5,570,035) disclose built-in self test indicator for an integrated circuit package.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HA T. NGUYEN can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VINH P NGUYEN
Primary Examiner
Art Unit 2829
10/26/06